APPLICATION FOR
UNITED STATES PATENT
IN THE NAME

Of

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For

ARCHITECTURE FOR HIGH THROUGHPUT SEMICONDUCTOR PROCESSING APPLICATIONS

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CROSS-REFERENCE TO RELATED APPLICATION

This application claims the benefit of and incorporates by reference U.S. Provisional Application No. 60/209,079, entitled "Wafer Transport And Processing System Architecture For High Throughput," filed on June 2, 2000, by Craig L. Stevens and Karl B. Levy.

BACKGROUND OF THE INVENTION

1. Field Of The Invention

The present invention relates generally to semiconductor device fabrication, and more particularly to semiconductor wafer processing systems.

2. Description Of The Background Art

Semiconductor wafer processing systems that have more than one module are referred to as "cluster tools." Typically, a cluster tool has a load lock module for receiving a semiconductor wafer, one or more process modules for performing fabrication steps on the wafer, and a transport module for moving the wafer from the load lock module to a process module, and vice versa. Exemplary cluster tools are disclosed in United States Patent No. 4,917,556 to Stark et al. and United States Patent No. 5,186,718 to Tepman et al., both of which are incorporated herein by reference in their entirety.

The arrangement of modules in a semiconductor wafer processing system (i.e., the system's architecture) directly affects throughput. Throughput is an important